

Two Approaches to 64-bit Computing

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May 12, 2003

Agenda

- Why 64-bit?
- Porting Issues
- Intel's Approach: IA-64
- AMD's Approach: x86-64
- Instruction Encoding
- Addressing Modes
- Registers
- Architecture comparison
- Itanium Branching
- 32-bit Compatibility
- Itanium vs. Hammer
- Scalability
- Questions

Why 64-bit?

- Larger word sizes allow:
 - Greater integer math precision
 - Larger virtual address space
 - 1.8×10^{19} bytes
- Handle very large data sets:
 - Large databases
 - Satellite images

Why 64-bit?

- Faster processing of parallel data
- Double bandwidth between register file and L1 cache
- Higher performance

Porting Software to 64-bit Platform

- Some 4 byte types change to 8 bytes
 - long (depending on platform)
 - 4 bytes on Windows compilers (LLP64 model)
 - 8 bytes on Linux/Unix compilers (LP64 model)
 - Pointers
 - sizeof
 - size_t
 - off_t

Porting Software to 64-bit Platform

- Most of the work is good coding practice
- Use `stdint.h` (C99 spec)
 - Defines fixed-size data types

AMD's approach: x86-64

- Extend the “standard” x86 instruction set to 64 bits
- Very similar to extension from 16- to 32-bit processors (286 to 386)

Intel's Approach: IA-64

- Design new Instruction Set Architecture from scratch
- Support 32-bit x86 programs through an Emulation Layer

ISA Paradigm

- IA-64
 - EPIC (Explicitly Parallel Instruction set Computing) architecture
 - superset of VLIW
- x86-64
 - CISC architecture

x86-64 modes

- Global control bit and code segment description flags are used to specify the operation mode of the CPU

LME	code segment flag		Mode
	L bit	D bit	
0	x	0	Legacy 16-bit mode
0	x	1	Legacy 32-bit mode
1	0	0	Compatibility 16-bit mode
1	0	1	Compatibility 32-bit mode
1	1	0	64-bit mode
1	1	1	Reserved

Addressing Modes

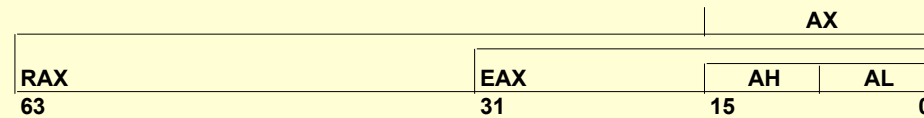
- IA-64

- register indirect

- x86-64

- absolute
- register indirect
- based
- indexed
- ...
- ...
- relative to program counter (RIP)

x86-64 Registers



x86-64 Registers

	In x86
	Added by x86-64

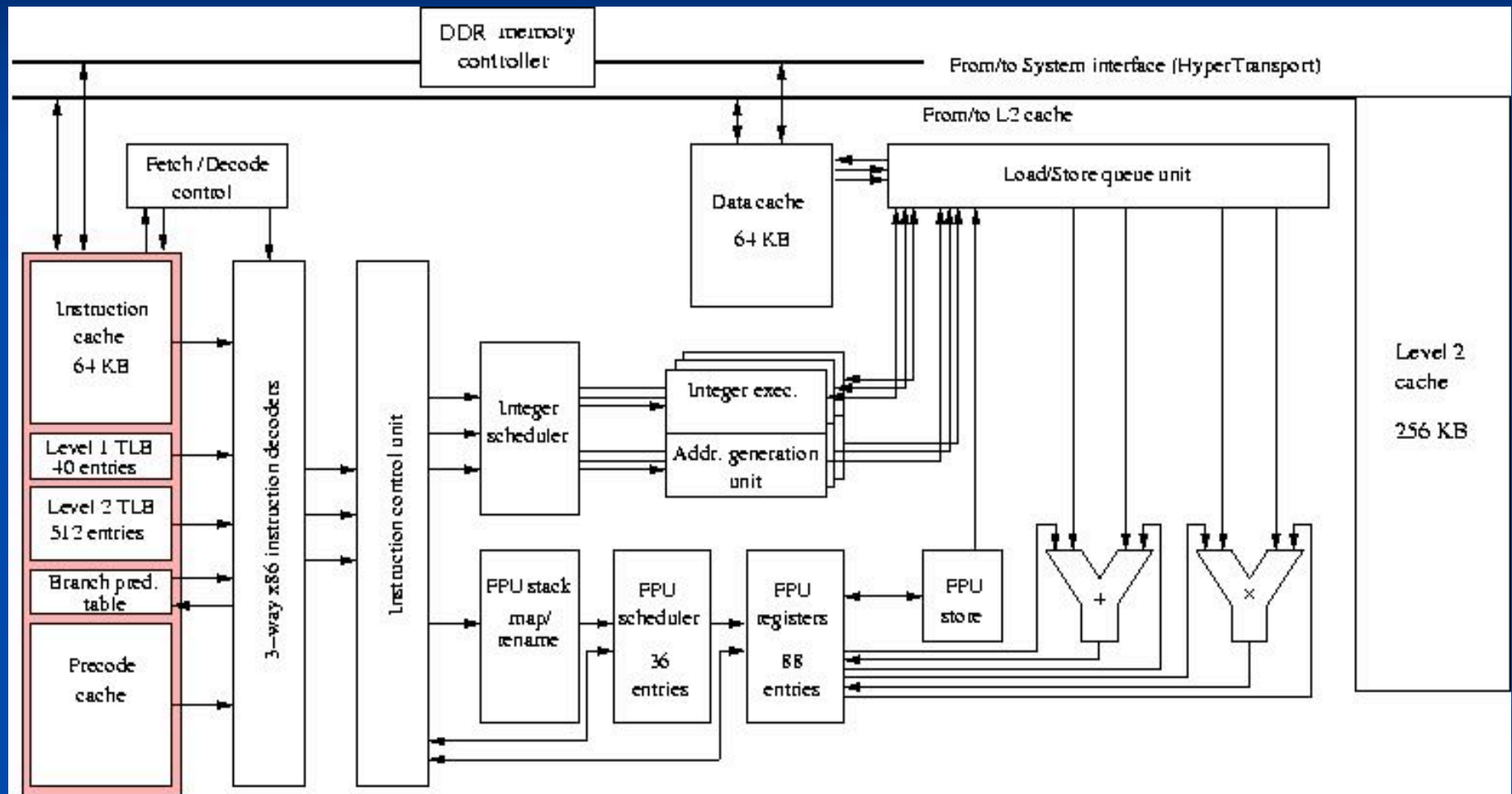
GPR		X87		SSE & SSE2	
RAX	EAX	MM0/ST0		XMM0	
RBX	EBX	MM1/ST1		XMM1	
RCX	ECX	MM2/ST2		XMM2	
RDX	EDX	MM3/ST3		XMM3	
RBP	EBP	MM4/ST4		XMM4	
RSI	ESI	MM5/ST5		XMM5	
RDI	EDI	MM6/ST6		XMM6	
RSP	ESP	MM7/ST7		XMM7	
R8				XMM8	
R9				XMM9	
R10				XMM10	
R11				XMM11	
R12				XMM12	
R13				XMM13	
R14				XMM14	
R15				XMM15	
63	0				

Program Counter	
RIP	EIP

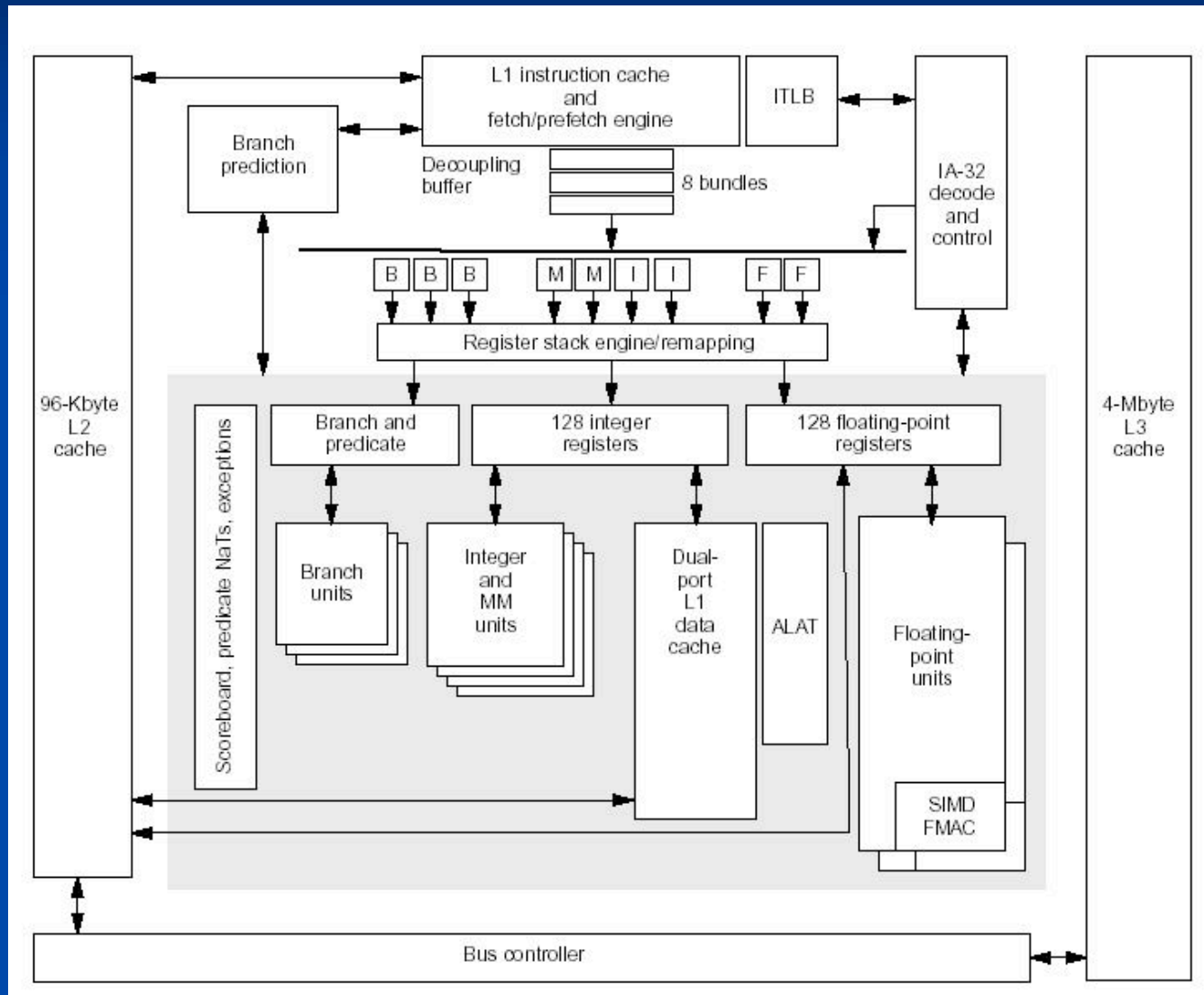
IA-64 Registers

- 128 general purpose
- 128 floating point
- Itanium contains dedicated hardware to rename and remap registers

Hammer Architecture



Itanium Architecture



Itanium Branching

- Branch hints

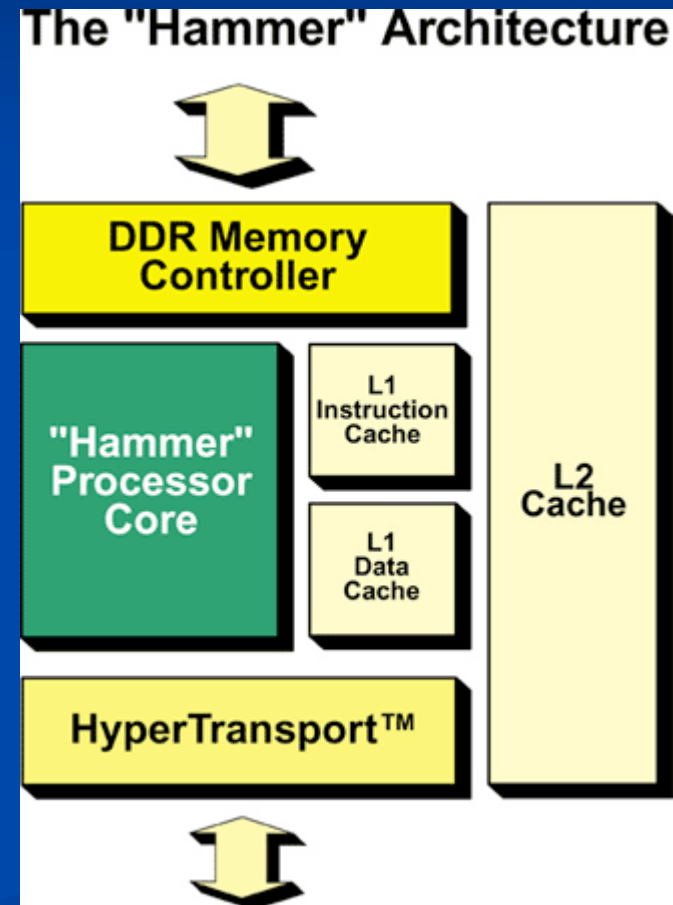
- Specific branch hint instruction: BPR
- All branching instructions have branch hint fields

- Predicates

- Almost all instructions can be predicated
- Turns a control dependency (branching) into a data dependency (predicates)
- Allows forwarding to solve some control hazards

Scalability

- Hammer
 - Integrated DDR DRAM memory controller
 - HyperTransport technology
- Itanium
 - 4-way glueless multiprocessing



32-bit Compatibility

- Itanium
 - Currently has hardware emulation of x86
 - Recently decided to instead include software in OS to translate IA-64 to x86
- Hammer
 - x86-64 is a superset of x86
 - 32-bit x86 programs are run natively

Itanium vs. Hammer

- 128 vs. 16 GPRs
- 128 FPRs vs. 8 FPRs and 16 SIMD registers
- Parallelism: compile-time vs. run-time
- Decoding: Fixed vs. Variable length
- Addressing Modes: 1 vs. many
- Address Generation Units: 0 vs. 3
- Execution Units: 4 Int, 2 FP vs 3 Int, 3 FP
- Cache: 3 levels vs. 2 levels

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